Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for checking optical proximity correction data, the method comprising:

(a) dividing a chip region into at least first and second regions;

(b) selecting the first region from the divided regions;

(c) providing a first layout database of an integrated circuit design corresponding to the first region, wherein the first layout database is obtained before optical proximity correction treatment;

(d) providing a second layout database of the integrated circuit design corresponding to the first region, wherein the second database is obtained after optical proximity correction treatment;

(e) finding a location of a first structure in the first layout database;

(f) simulating a resulting layout output for the first structure using the second layout database;

(g) measuring a first critical dimension of the first structure from the resulting layout output for the first structure;

(h) comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; ~~and~~

(i) flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension of the first database;

(j) repeating the steps (a) to (i) to generate a defect report at least on the first and second regions;

(k) analyzing the defect report to identify one or more problematic patterns; and

(l) identifying unique patterns from the one or more problematic patterns.

2. (Currently amended) The method of claim 1 wherein ~~the step of flagging the first structure in the second database if the first dimension is less than the first drawn dimension in the first database~~ the step (i) is replaced by flagging the first structure in the second database if the first dimension is less than the first drawn dimension plus a tolerance value in the first database.

3. (Currently amended) The method of claim 2 wherein the tolerance value is defined by a user.

4. (Original) The method of claim 1 wherein the first and second layout databases in GDSII format.

5. (Original) The method of claim 1 wherein the first structure is at least one of a transistor gate, transistor end-cap line, line-end, via and gap, or contact and gap.

6. (Original) The method of claim 1 wherein the step of finding a location of a first structure in the first layout database is performed using pattern recognition.

7. (Original) The method of claim 1 wherein when the first structure is a transistor gate, the first critical dimension is a gate length.

8. (Original) The method of claim 1 wherein the first structure is a transistor gate, the first critical dimension is a gate width.

9. (Currently amended) The method of claim 1 further comprising:

(m) building a model of a process, to be used to fabricated the integrated circuit design, and wherein the step of simulating a resulting layout output for the first structure using ~~he~~ the second layout database is performed using this model of the process.

10. (Original) The method of claim 1 wherein the step of simulating a resulting layout output for the first structure using the second layout database comprises consulting a look-up table.

11-13. (Canceled)

14. (Original) The method of claim 13 wherein the tolerance value is specified by a user.

15. (Currently amended) A method for generating a circuit design, the method comprising:

providing a first layout database of an integrated circuit design, wherein the first layout database is obtained before optical proximity correction treatment;

providing a second layout database of the integrated circuit design, wherein the second database is obtained after optical proximity correction treatment;

finding a location of a first structure in the first layout database;

finding a first structure in the second layout database based on its location in the first layout database;

simulating a resulting layout output for the first structure using the second layout database;

measuring a first critical dimension of the first structure from the resulting layout output for the first structure;

comparing the first critical dimension of the first structure to a drawn dimension of the first structure from the first database; ~~and~~

flagging the first structure in the first database if the first critical dimension is less than the first drawn dimension in the first database to generate a defect report;

analyzing the defect report to identify one or more problematic patterns; and

identifying unique patterns from the one or more problematic patterns.

16. (Original) The method of claim 15 further comprising:

flagging the first structure in the second database if the first critical dimension is less than the first drawn dimension in the first database.